CSc.111-2077 ✡

Tribhuvan University
Institute of Science and Technology
2077

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Bachelor Level / First Year/ First Semester/ Science
Computer Science and Information Technology (CSc. 111)
(Digital Logic)
(NEW COURSE)

Full Marks: 60
Pass Marks: 24
Time: 3 hours.

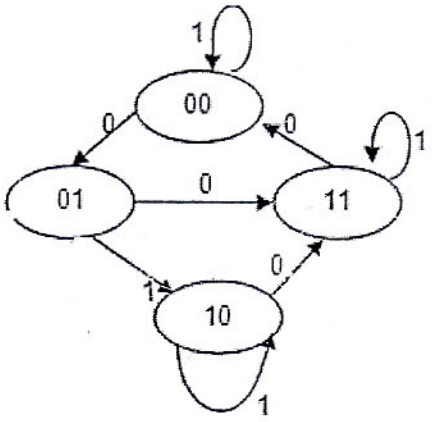
Candidates are required to give their answers in their own words as for as practicable.
The figures in the margin indicate full marks.

Attempt any two questions: (2×10=20)

1. Design a combinatorial circuit that generates 9's complement of a BCD number. (10)

2. Implement the following functions using PLA (10)
   w (A, B, C, D) = ∑(2,12,13)
   x (A, B, C, D)= ∑ (7,8,9,10,11,12,13,14,15)
   y (A, B, C, D) = ∑ (0,2,3,4,5,6,7,8,10,11,15)
   z (A, B, C, D) = ∑ (1,2,8,12,13)

3. Design sequential circuit specified by the following state diagram using T flip-flops. (10)



4. List two major characteristics of digital computer. Represent -6 (negative six) using 8 bits in signed magnitude, signed-1's-complement and signed-2's-complement respectively. Represent decimal number 4673 in a) octal, and b) BCD. (1+2+2)

5. Where is CMOS suitable to use? Define Power dissipation. Show that the positive logic NAND gate is a negative logic NOR gate and vice versa. (1+1+3)

6. Simplify the following function and implement them with two level NOR gate circuit, F(w, x, y, z) = $wx' + y'z' + w'yz'$ (5)

7. Design a full subtractor circuit with three inputs x, y, B_{in} and two outputs Diff and B_{out}. The circuit subtracts x-y-B_{in} where B_{in} is the input borrow, B_{out} is the output borrow, and Diff is the difference. (5)

8. Design 4-bit even parity generator. (5)

9. What is the difference between a serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed? (1+3+1)

10. Explain negative-edge triggered D flip flop with necessary logic diagram and truth table. (5)

11. Illustrate the use of Binary ripple counter and BCD ripple counter. (2.5+2.5)

12. Write Short notes on (Any two) (2x2.5)

    a) RTL
    b) State Reduction
    c) POS