Tribhuvan University

Institute of Science and Technology

2081

*

Bachelor Level / First Year/ First Semester/ Science

Computer Science and Information Technology (CSC 116)

(Digital Logic)

Pass Marks: 24 Time: 3 hours.

Full Marks: 60

(NEW COURSE)

Candidates are required to give their answers in their own words as for as practicable. The figures in the margin indicate full marks.

Section A

Attempt any TWO questions.

 $(2 \times 10 = 20)$

- 1. Design a combinational circuit with three inputs and one output.

 The output is 1 when binary value of the inputs is less than or equal to 3. The output is 0 otherwise.
- 2. Design the sequential circuit whose state table is given below using a 2-bit register and combinational gates. (10)

Present	State	Input	Next	state
A	В	X	A	В
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1 .	0
1	0	1	1	1-
1	1	0	1	0
1	. 1	1	0	1

3. Implement $F = \Sigma(1, 3, 4, 5, 7)$ using

(4+6)

- a) Multiplexer
- b) PLA

IOST TH

Section B

Attempt any EIGHT questions.		
4.	Perform the following conversion a) (A57) ₁₆ to binary b) (110001) ₂ to octal	(2.5+2.5)
5.	Differentiate between BCD and Gray code. Convert (10) ₁₀ to BCD.	(3+2)
6.	Simplify the Boolean Function products of sum using the don't-care conditions d $F = w'(x'y + x'y' + xyz) + x'z'(y + w)$ $d = w'x(y'z + yz') + wyz$	(5)
7.	What is decoder circuit? Design 3 to 8 decoder circuit.	(5)
8.	Explain the concept of bidirectional shift register with parallel load.	(5)
9.	What are the special characteristics of IC digital logic family? Explain them in brief	f. (5)

CSC116-2081(New)☆

10. Express the Boolean Function F = AB' + BC in a sum of min terms. (5)

11. Describe the working mechanism of edge triggered flip flop? What are its advantages? (3+2)

12. Write short notes on

(2.5+2.5)

a) Latch

b) Memory