Tribhuvan University
Institute of Science and Technology
2081
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Bachelor Level / First Year/ First Semester/ Science
Computer Science and Information Technology (CSC 111)
(Digital Logic)
(OLD COURSE)

Full Marks: 60
Pass Marks: 24
Time: 3 hours.

Candidates are required to give their answers in their own words as for as practicable.
The figures in the margin indicate full marks.

Section A

Attempt any TWO questions. **(2×10=20)**

1. Describe asynchronous counter. Explain binary ripple counter. [2+8]

2. Implement $F = \Sigma(0, 2, 3, 5, 6)$ using [4+6]
   a) Decoder
   b) PAL

3. Design a combinational circuit that accepts a three bit number and generates an output number equal to the square of the input number. [10]

Section B

Attempt any EIGHT questions. **(8×5=40)**

4. Perform the following conversion [2.5+2.5]
   a) $(145.02)_{10}$ to binary
   b) $(987)_{16}$ to decimal

5. Design 4 bit even parity generator. [5]

6. How parallel data is converted to serial data and parallel data to serial? Explain with respect to required register. [5]

7. Explain T flip flop. How is it different from SR flip flop? [4+1]
8. Define basic gates, derived gates and universal gates. Illustrate the use of universal gates. [3+2]
9. Simplify the following using k-map where d stands for don't care. [5]
   $F(A, B, C, D) = \Sigma(0, 1, 2, 8, 9, 12, 13)$
   $d(A, B, C, D) = \Sigma(10, 11, 14, 15)$

10. Design a half subtractor circuit using only NAND gates. [5]

11. Differentiate between multiplexer and demultiplexer. [5]

12. Write short notes on [2.5+2.5]
    a) State diagram
    b) Signed binary number