Tribhuvan University

Institute of Science and Technology

2080

✡

Bachelor Level / First Year/ First Semester/ Science

Computer Science and Information Technology (CSC 116)

(Digital Logic)

(NEW COURSE)

Full Marks: 60
Pass Marks: 24
Time: 3 hours.

Candidates are required to give their answers in their own words as for as practicable.

The figures in the margin indicate full marks.

Section A

Attempt any TWO questions. **(2×10=20)**

1. What is combinational circuit? Design a combinational circuit with four inputs lines that represent a decimal digit in BCD and four output lines that generate the 1's complement of the input binary patterns.

2. What is asynchronous counter? Design synchronous counter that counts the sequences of 0-1-4-6-7 using T flip-flop.

3. Implement the Boolean function $F(P,Q,R,S)= \Sigma (3,4,6,8,9,14)$ using:
   a. 8 to 1 multiplexer
   b. PLA
   c. Decoder

Section B

Attempt any EIGHT questions. **(8×5=40)**

4. Perform the following operations:
   a. $(011101)_2$-$(110011)_2$ using 2's complement
   b. $(89344)_{10}$-$(98654)_{10}$ using 9's complement

5. If $f(P,Q,R,S)= \Sigma (3,4,7,8,14)$ and $d(P,Q,R,S)= \Sigma(1,6,9,13)$. Simplify it using K-map and design circuit using minimum number of NAND gates.

6. What is drawback of RS Flipflop? Explain D Flip Flop in detail with Logic Diagram, characteristics table and Characteristics equation.

7. Design a full subtractor with necessary tables and logic diagram.

8. What is shift register? Explain 4-bit SISO and PIPO with timing Diagram.

9. Design an asynchronous Mod 11 up counter using T flip flop.

10. How race condition in JK flip flop can be resolved? Explain.

11. What is decoder circuit? Design 3 to 8 decoder circuit.

12. Write short notes on:
    a. State Diagram
    b. Encoder
    c. Parallel Adder