Tribhuvan University
Institute of Science and Technology
2081
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Bachelor Level / First Year/ First Semester/ Science
Computer Science and Information Technology (CSc. 111)
(Digital Logic)
(OLD COURSE)

Full Marks: 60
Pass Marks: 24
Time: 3 hours.

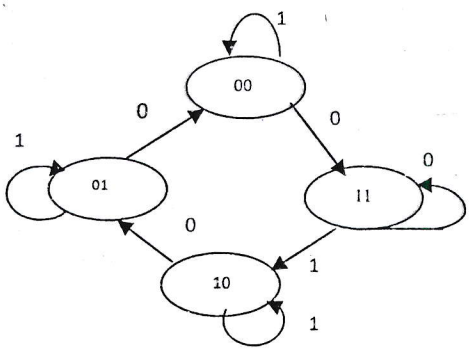
Candidates are required to give their answers in their own words as for as practicable.
The figures in the margin indicate full marks.

Section A

Attempt any TWO questions. **(2×10=20)**

1. Implement the following function $F = \sum(0,1,3,5,7)$ using
   a) Decoder
   b) Multiplexer
   c) PLA

2. Design clocked sequential circuit of the following state diagram by using RS flip-flop.



3. Implement full adder using Decoder and an OR gate. Explain its working mechanism.

Section B

Attempt any EIGHT questions. **(8×5=40)**

4. Represent decimal number 8620 in
   a) BCD
   b) Excess-3 code
   c) 2421 code
   d) Binary number

5. Express the Boolean function F = xy+x 'z in product of maxterm form.

6. Reduce the following function using k-map.
   F=A'D + BD + B'C + AB'D

7. Design a combinational circuit that adds one to a 4- bit binary number, $A_3A_2A_1A_0$. For example, if the input of the circuit is $A_3A_2A_1A_0$ = 1101, the output is 1110. The circuit can be designed using four half-adders.

8. Draw a logic diagram of a 2-to-4-line decoder with only NOR gates. Include an enable input.

9. Design the odd parity generator circuit.

10. Draw parallel-in parallel-out shift registers. Explain them.

11. Design a 4-bit binary synchronous counter with D flip-flops.

12. Write short notes on (Any two)
    a) Reflected code
    b) CMOS
    c) Don't care