Digital System Design

Course Title: Digital System Design
Course No: CSC417
Nature of the Course: Theory + Lab
Semester: VII

Full Marks: 60 + 20 + 20
Pass Marks: 24 + 8 + 8
Credit Hrs: 3

Course Description:
This course contains the introductory part of combinational Logic along with the clear concepts of K-Maps and Quine- Mc Cluskey Method. It also introduces sequential networks with flip flops and FSM. Another concept includes FPGA and VHDL and also testing and verification.

Course Objective:
The course objective is to provide ample knowledge on digital design process and to enhance the knowledge of hardware design in real scenarios.

Course Content:

Unit 1	Introduction of logic design, Digital System and Integration, Electronic Design Automation, IC Manufacturing, Logic Families, IC Design Techniques, IC characteristics: fan-out, power dissipation, propagation delay, and noise margin of TTL and CMOS integrated circuit logic devices	5Hrs
Unit 2	Review of Boolean Algebra and Combinational Logic, Canonical Form, Shannon's Expansion, Minterms, Maxterms, Prime Implication	4 Hrs.
Unit 3	Combinational Network Design: K – Map, Synthesis and Minimization with K – Maps (AND – OR, OR-AND, NAND-NAND, NOR-NOR), Standard Combinational Networks	5 Hrs.
Unit 4	Quine- Mc Cluskey Method, Minimization of Boolean expression with Quine-Mc Cluskey method, PROMs and EPROMs, Programmable Array Logic (PAL), Programmed Logic Array (PLA), Gate Arrays, Programmable Gate Array, Full Custom Design	7 Hrs.
Unit 5	Sequential Networks: Transition from combinational to sequential network, Direct command flip flop, Initialization of sequential network, Level Enabled Flip-Flops, Synchronization of sequential networks, Edge-triggered Flip Flops, Synchronous and Asynchronous Signals	8 Hrs.
Unit 6	Sequential Networks as Finite State Machines: Standard Models, Realization with ASM Diagrams, Synthesis of Synchronous FSM, Time	6 Hrs.

	Behavior of Synchronous FSM, Design of input forming, Logic and Output Forming Logic of state machine.	
Unit 7	Field Programmable Gate Arrays (FPGA), VHDL and its use in programmable logic devices (PLDs) like FPGA	4 Hrs.
Unit 8	Testing and Verification, Testing Logic Circuits, Combinational gate testing, Combinational network testing, Sequential Testing, Test vector generation, fault, fault model and fault detection, SA0, SA1, Design for Testability	6 Hrs.

Laboratory Works:
Laboratory Exercise should cover the implementation of combinational and sequential circuits, FSM, FPGA and VHDL. Testing and verification of circuits.

Project Work:
Design a sample of tool kit by using the design concepts of the course.

Reference Books:

1. Giuliano Donzellini, Luca Oneto, Domenico Ponta, Davide Anguita, Introduction to Digital System Design, Springer
2. Wolf, Wayne, Modern VLSI Design-System on Silicon, Third Edition, Pearson
3. Comer, David J. Digital Logic State Machine Design, Third Edition, Oxford University Press
4. Ashenden, Peter J, The Student's Guide to VHDL, Morgan Kaufman